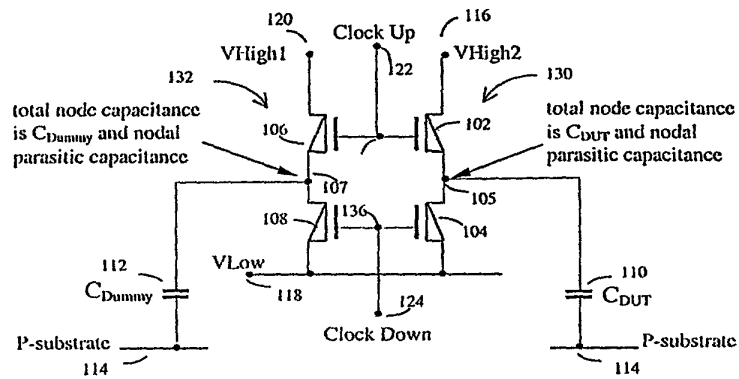


FIG. 1



100

FIG. 2

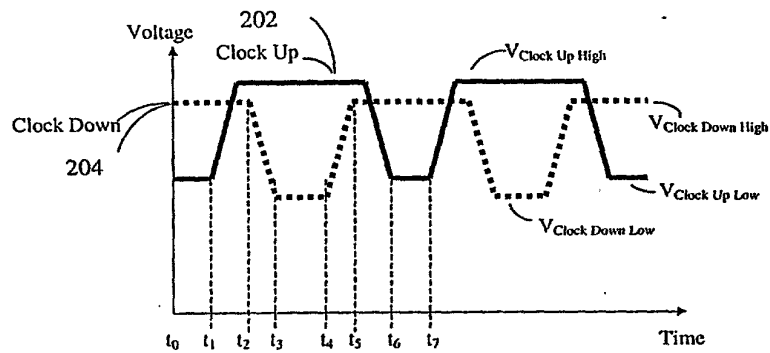


FIG.3

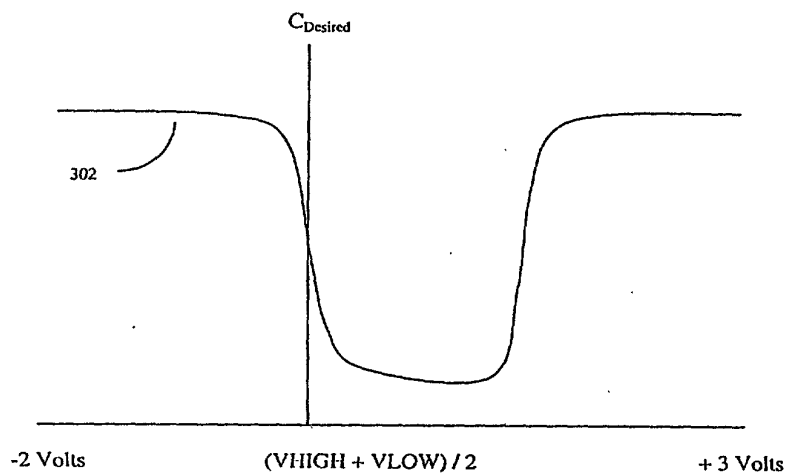


FIG. 4

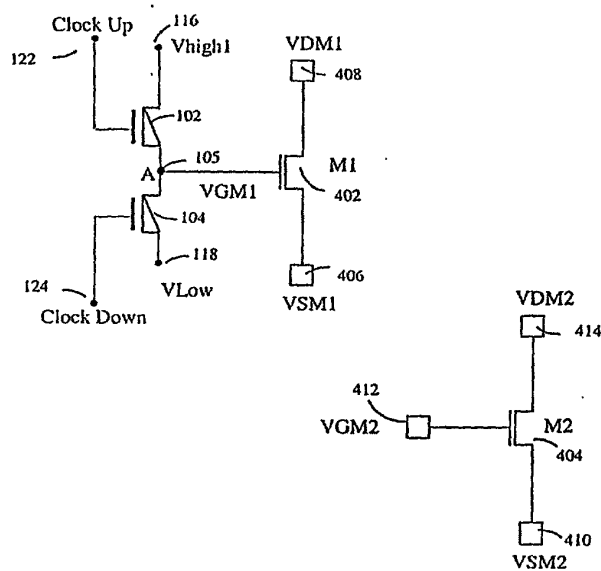
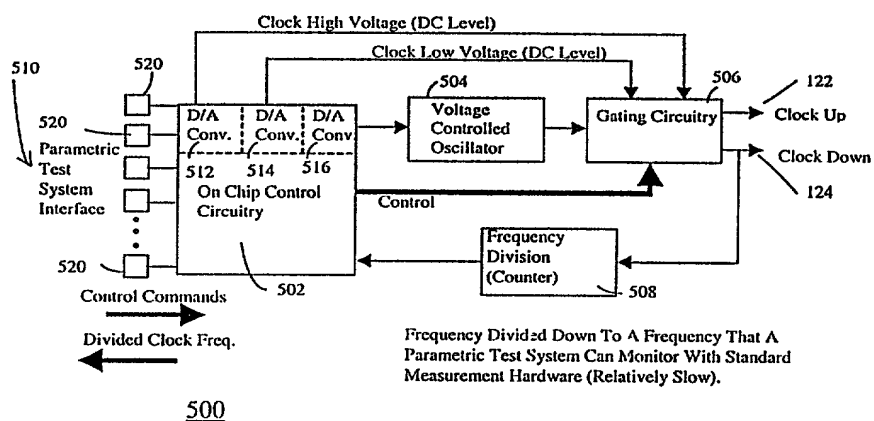
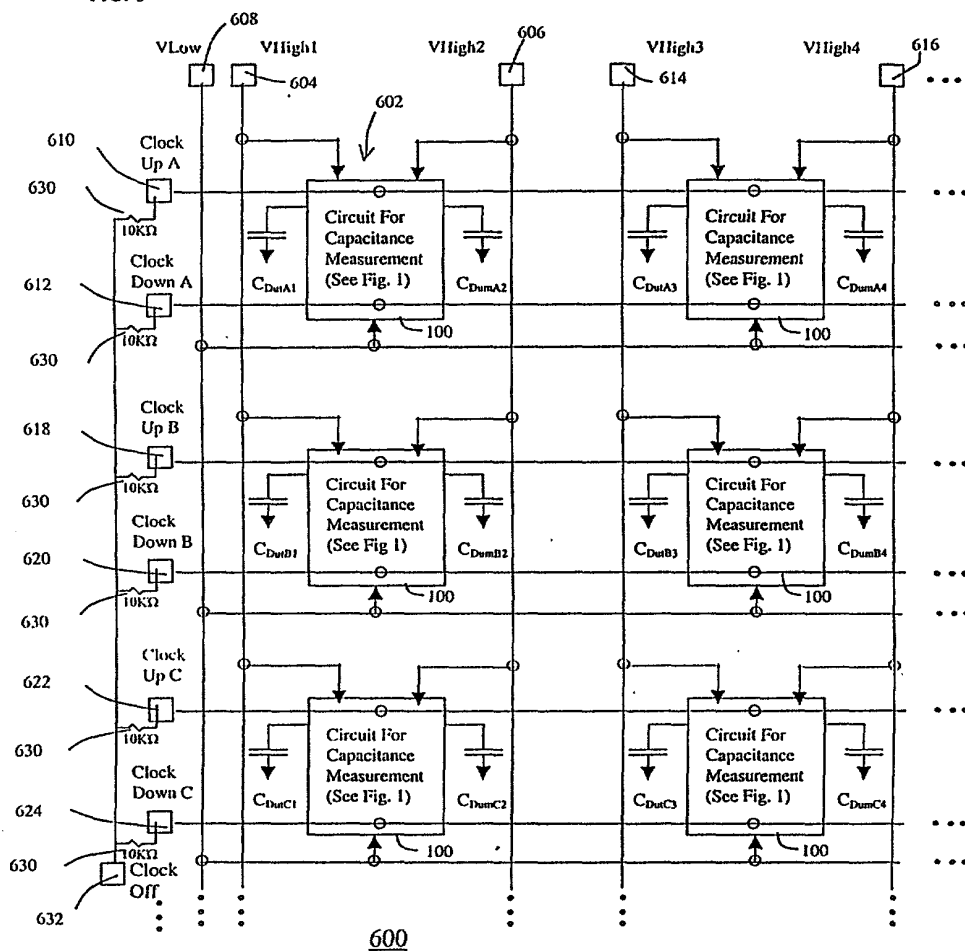


FIG. 5



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FIG. 6



600

FIG. 8

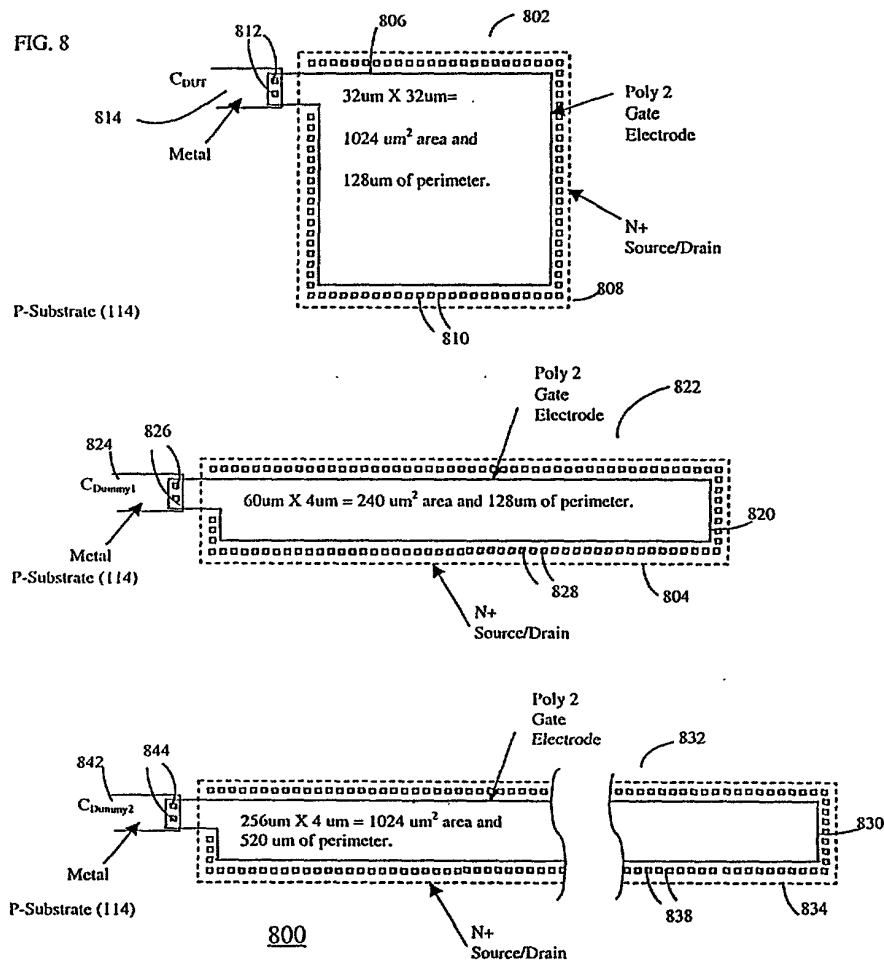
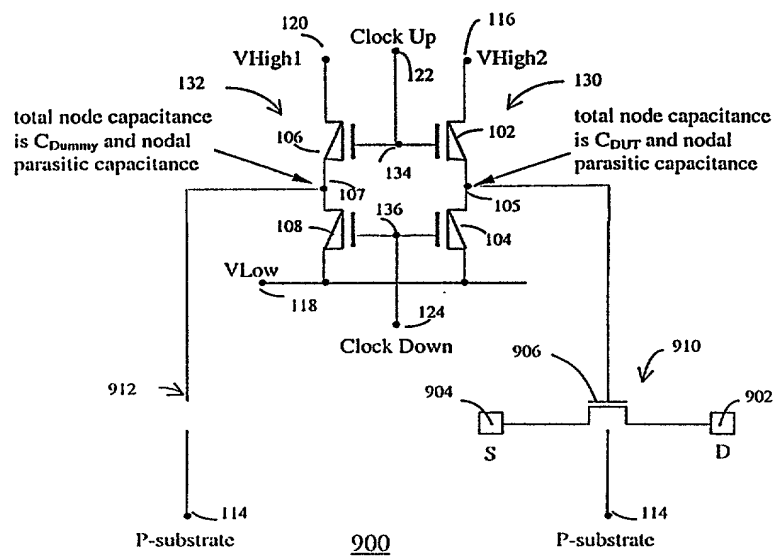
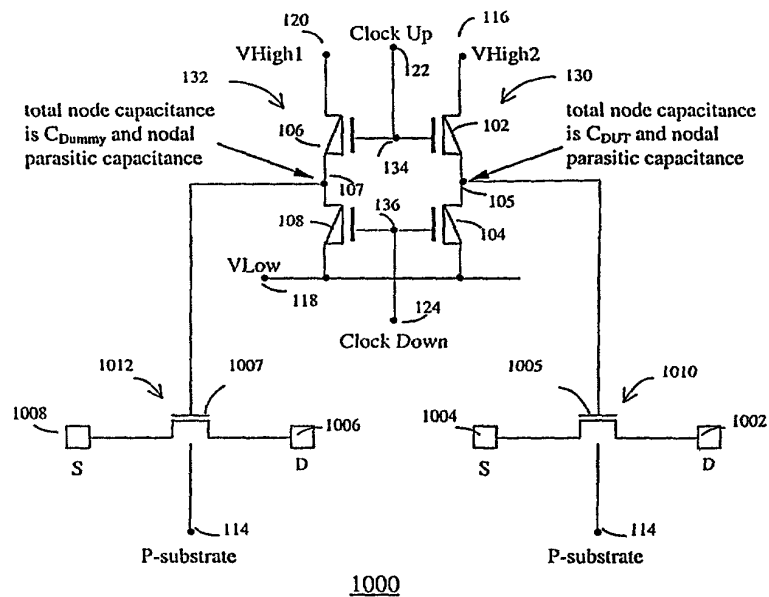


FIG. 9



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FIG. 10



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FIG. 11

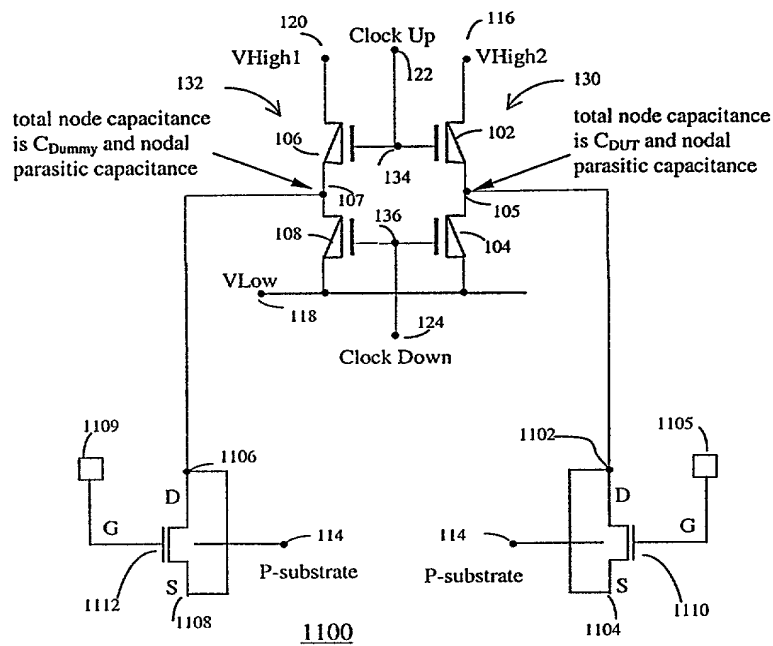


FIG. 12

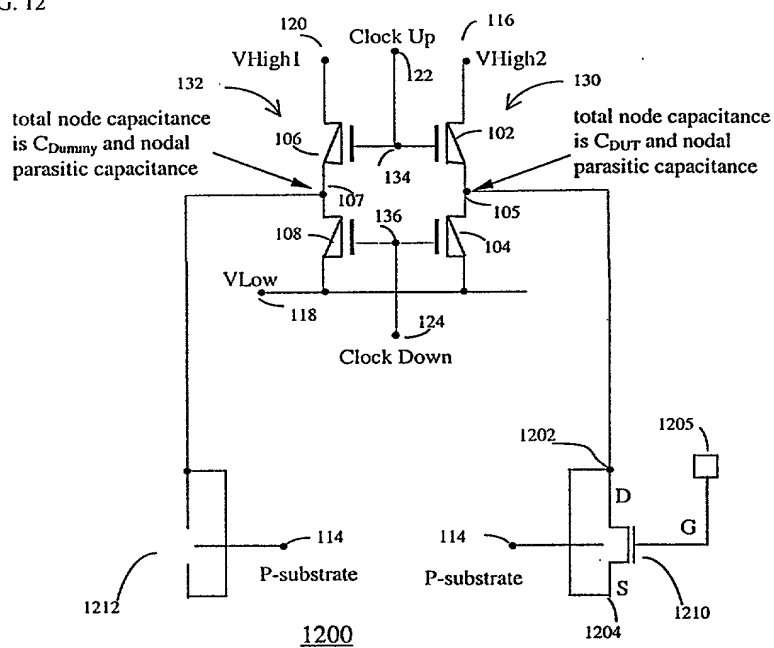
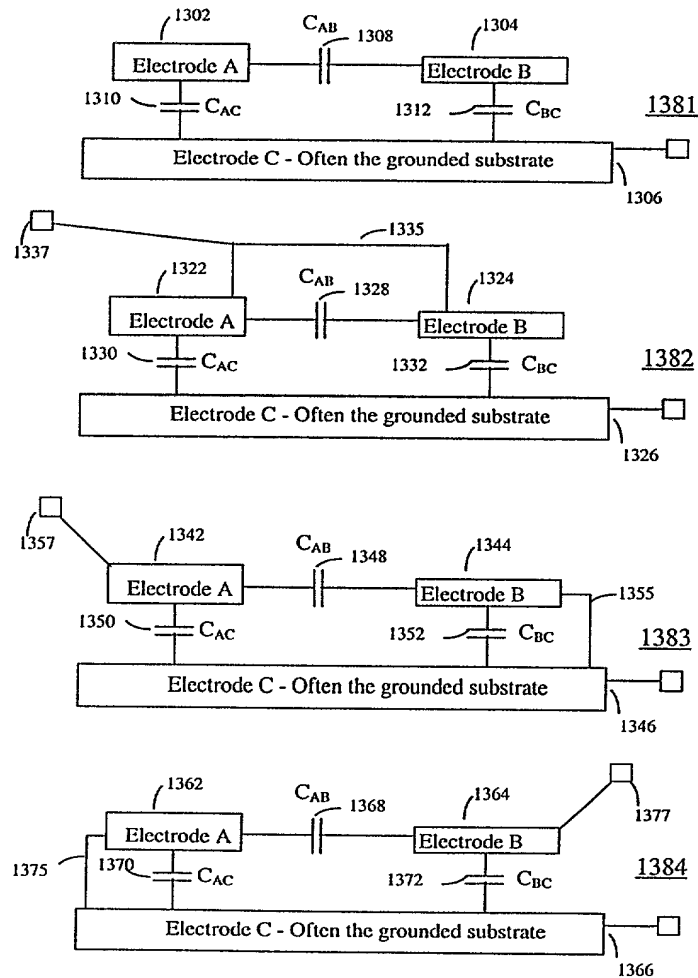
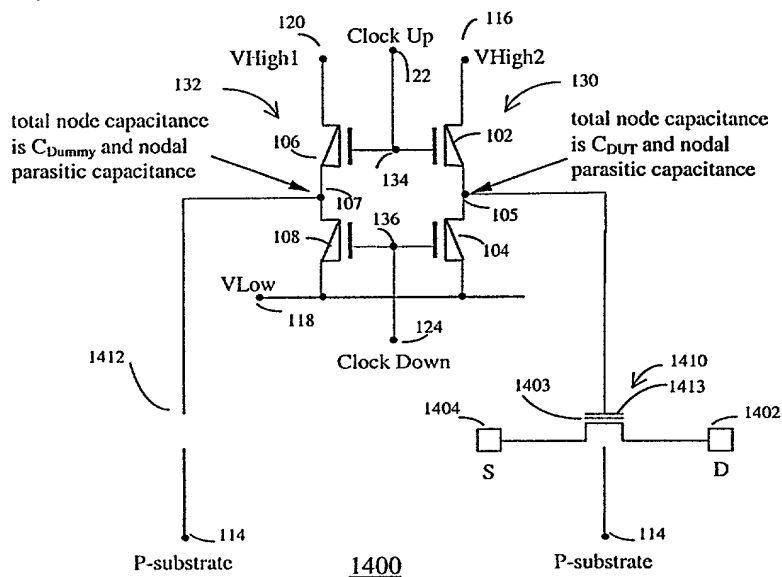


FIG. 13



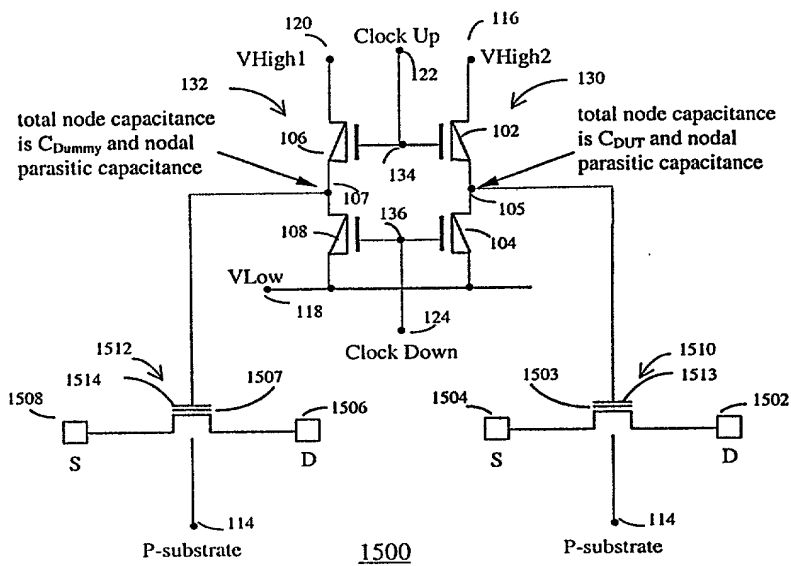
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FIG. 14



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FIG. 15



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FIG. 16

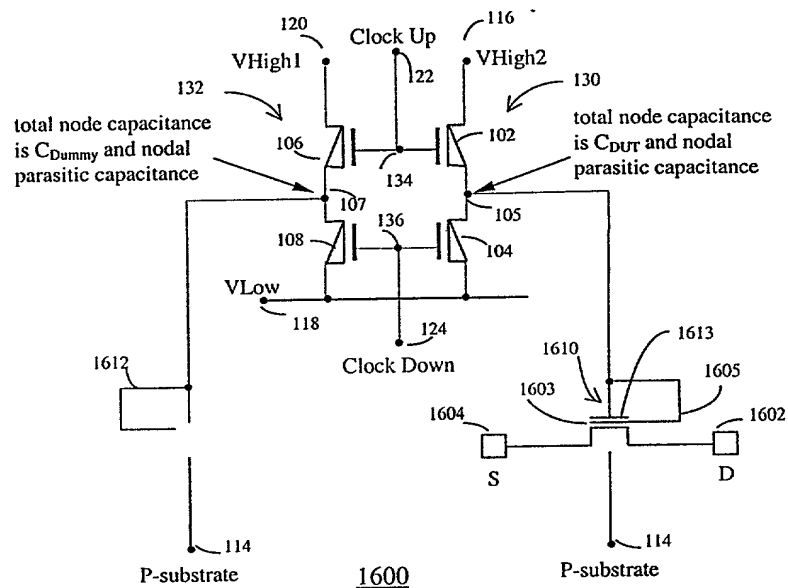
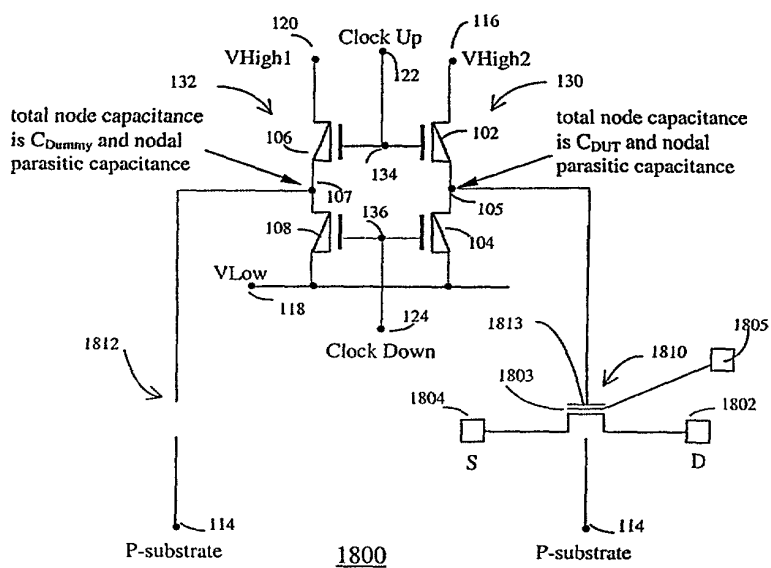


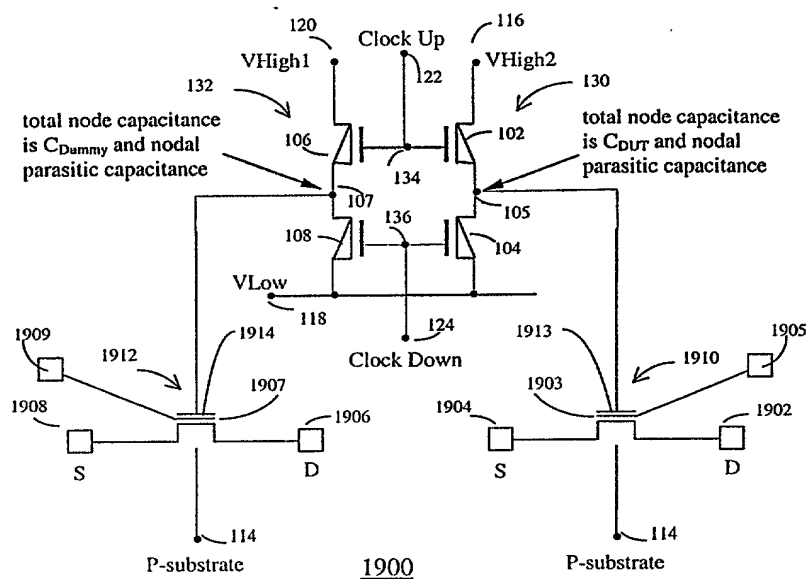


FIG. 18



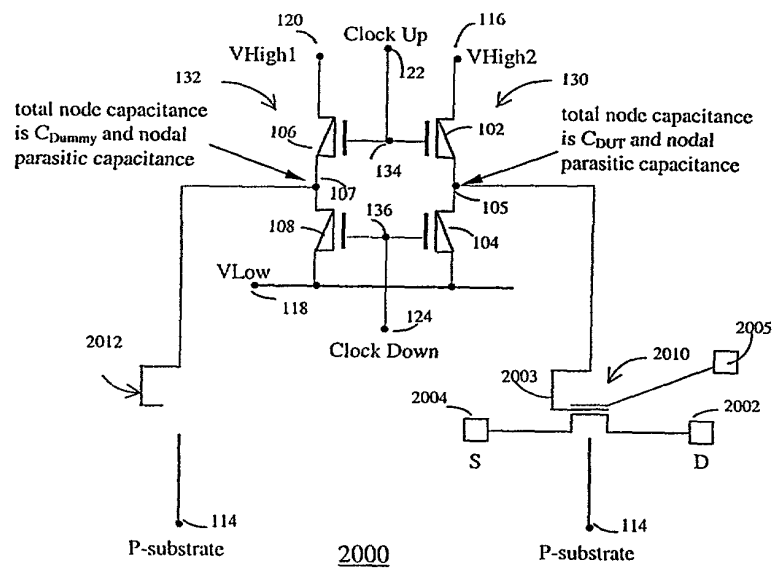
19/38

FIG. 19



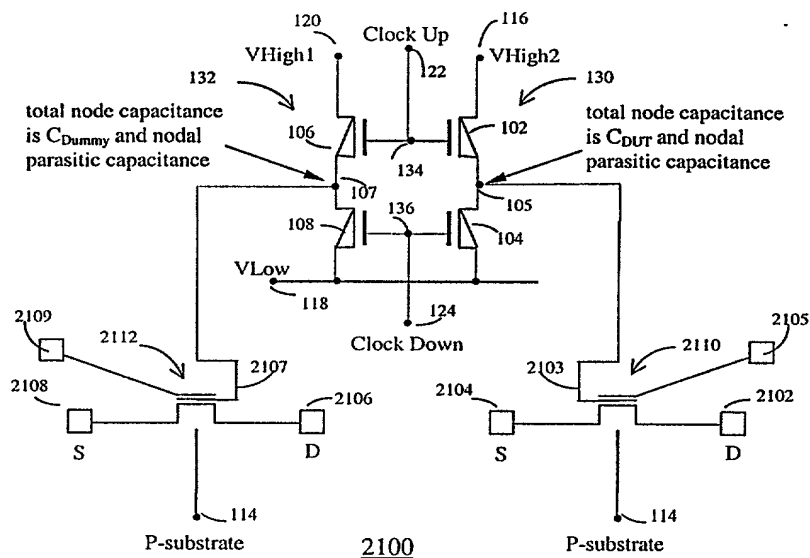
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FIG. 20



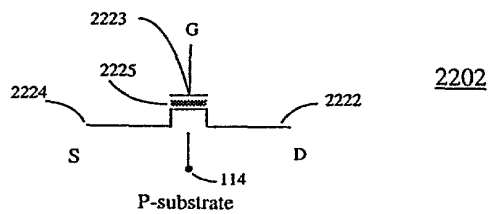
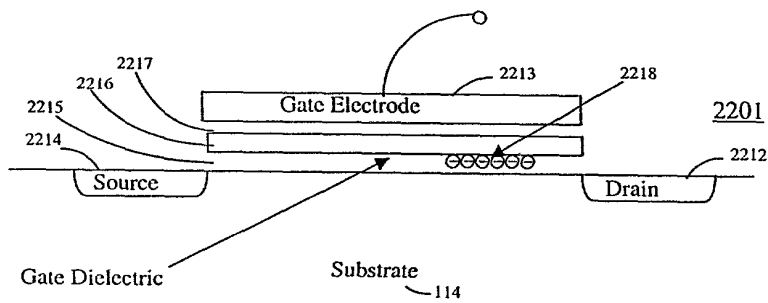
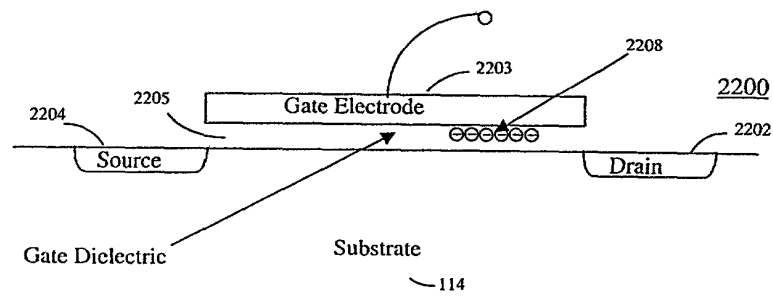
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FIG. 21



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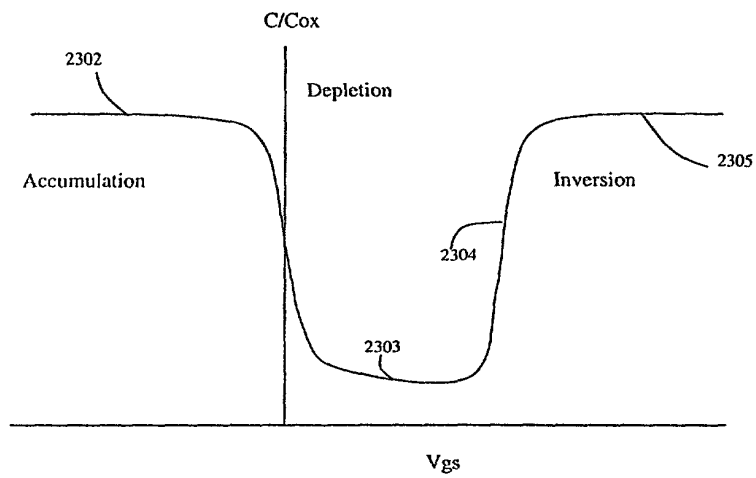
FIG. 22



Patent Application for: CLOCKED BASED METHOD AND DEVICES FOR MEASURING VOLTAGE-VARIABLE
CAPACITANCES AND OTHER ON-CHIP PARAMETERS
Inventor(s): David Michael Rogers, et al.
Attorney Docket No.: 9076/70

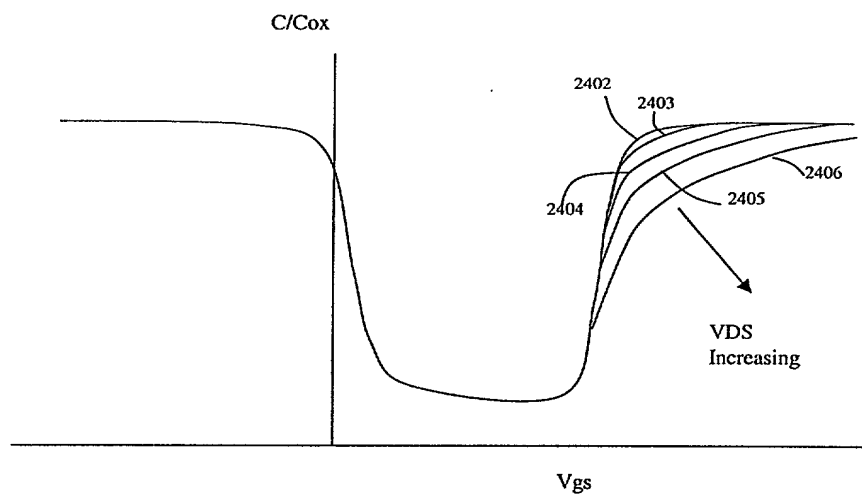
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FIG. 23:



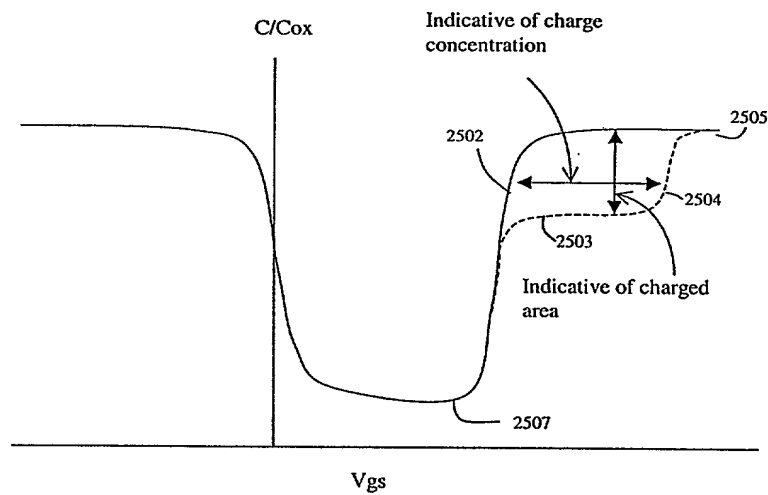
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FIG. 24



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FIG. 25



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FIG. 26

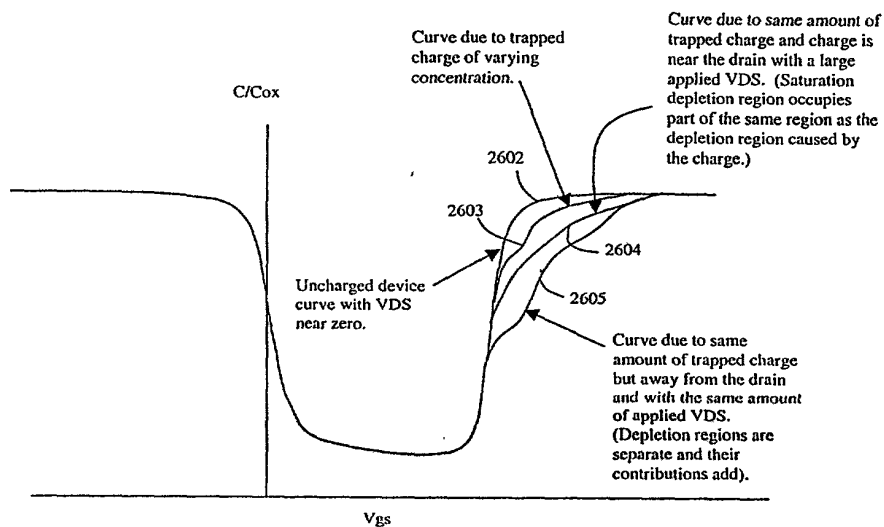
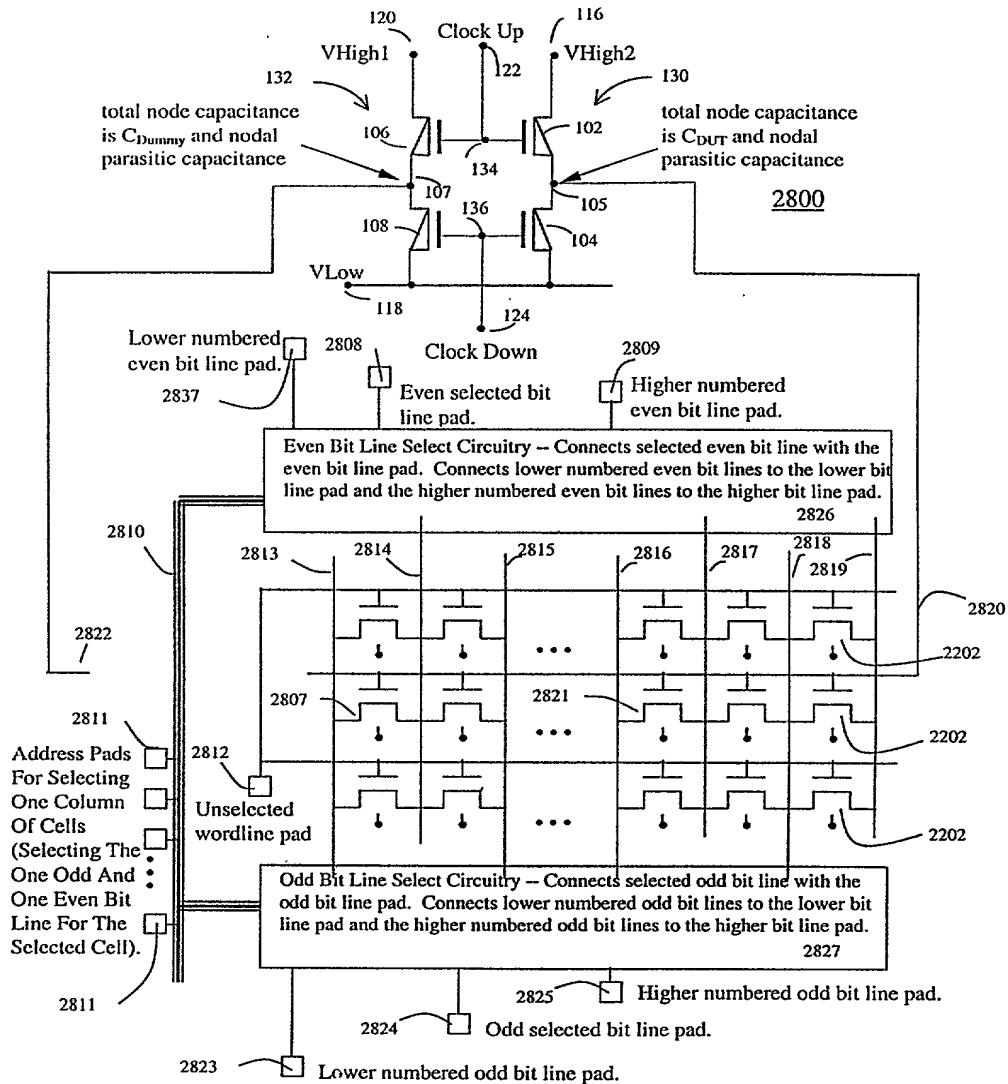


Figure 1 is a schematic diagram of a differential signal output circuit 2700. The circuit includes a differential pair of PMOS transistors 102 and 104, and NMOS transistors 106 and 108. The PMOS gates are connected to a "Clock Up" signal 120, and the NMOS gates are connected to a "Clock Down" signal 124. The PMOS sources are connected to VHigh1 122 and VHigh2 116, and the NMOS sources are connected to VLow 118. The drains are connected to a differential load 2702, which includes capacitors 2202 and is connected to a P-substrate 114. The output nodes are labeled 2713 and 2717. The total node capacitance is noted as C_{Dummy} and nodal parasitic capacitance.

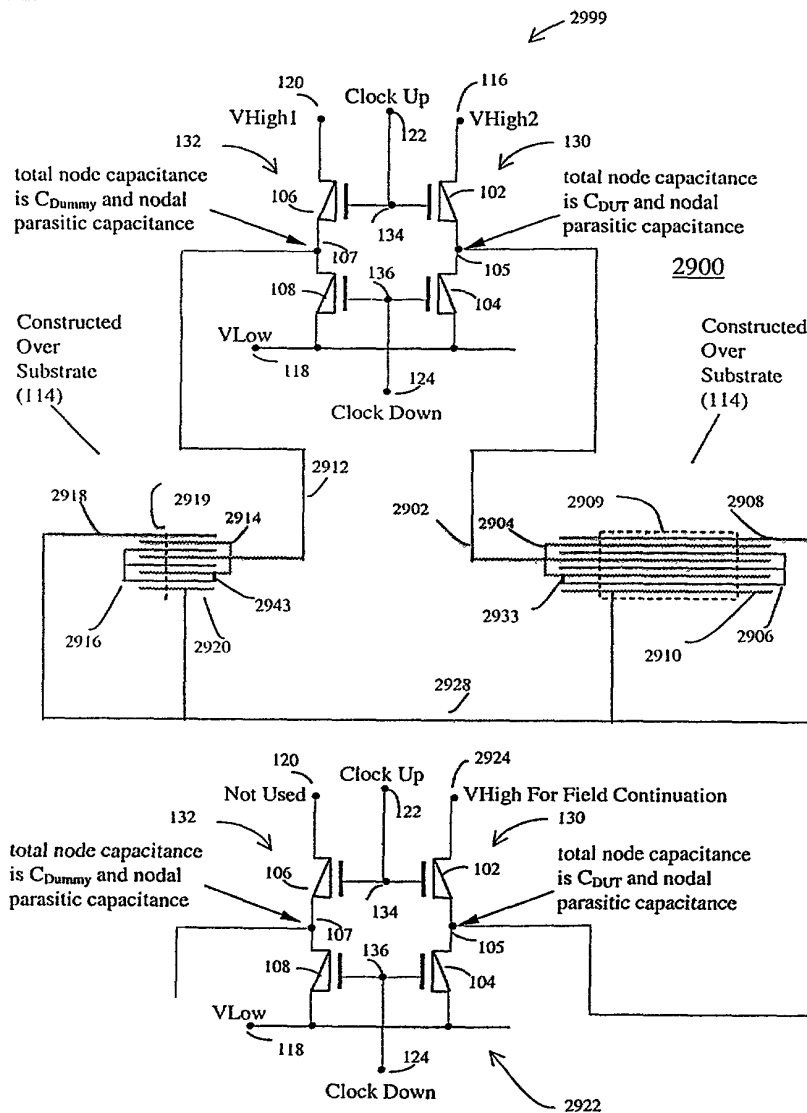
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FIG.28



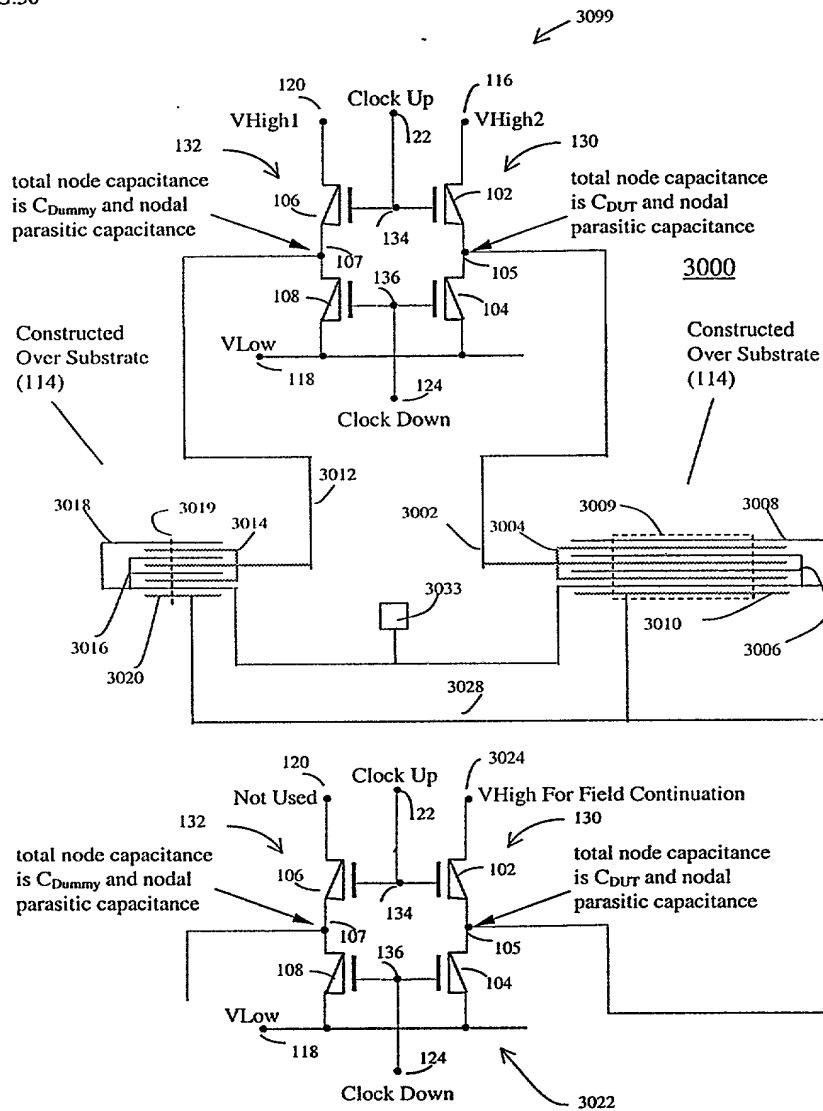
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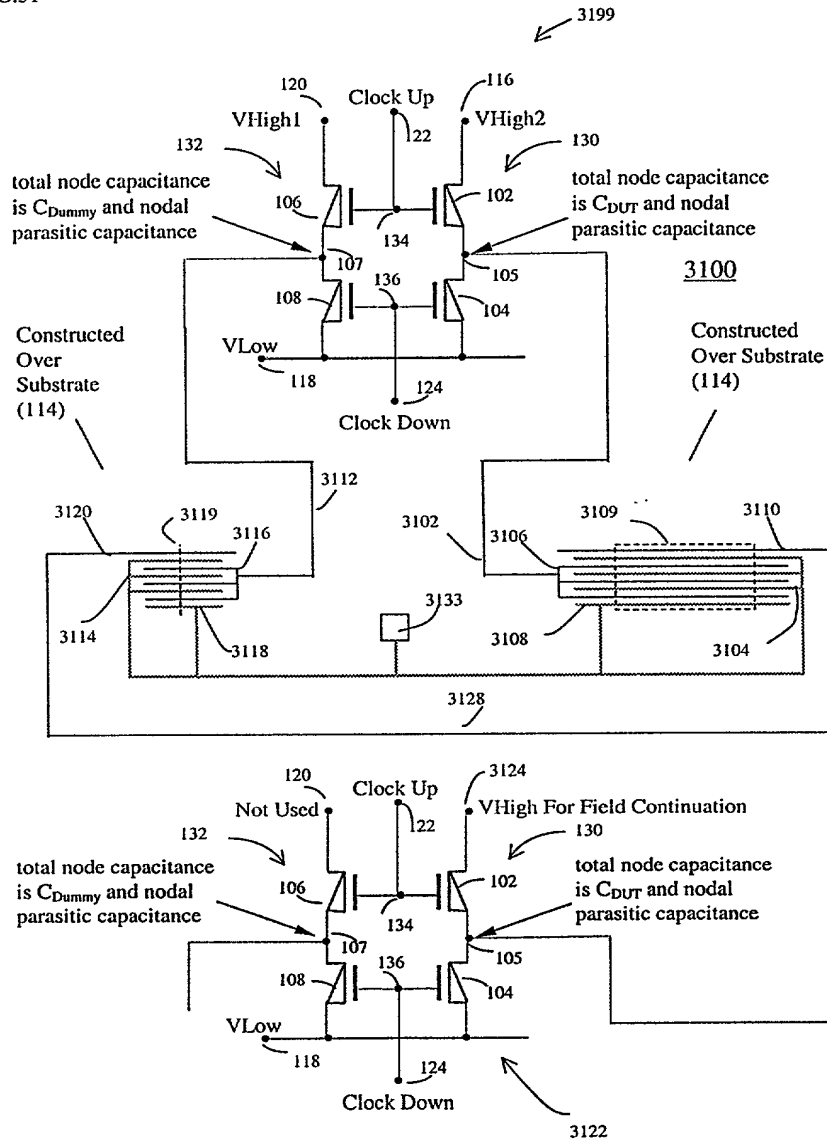
FIG.29



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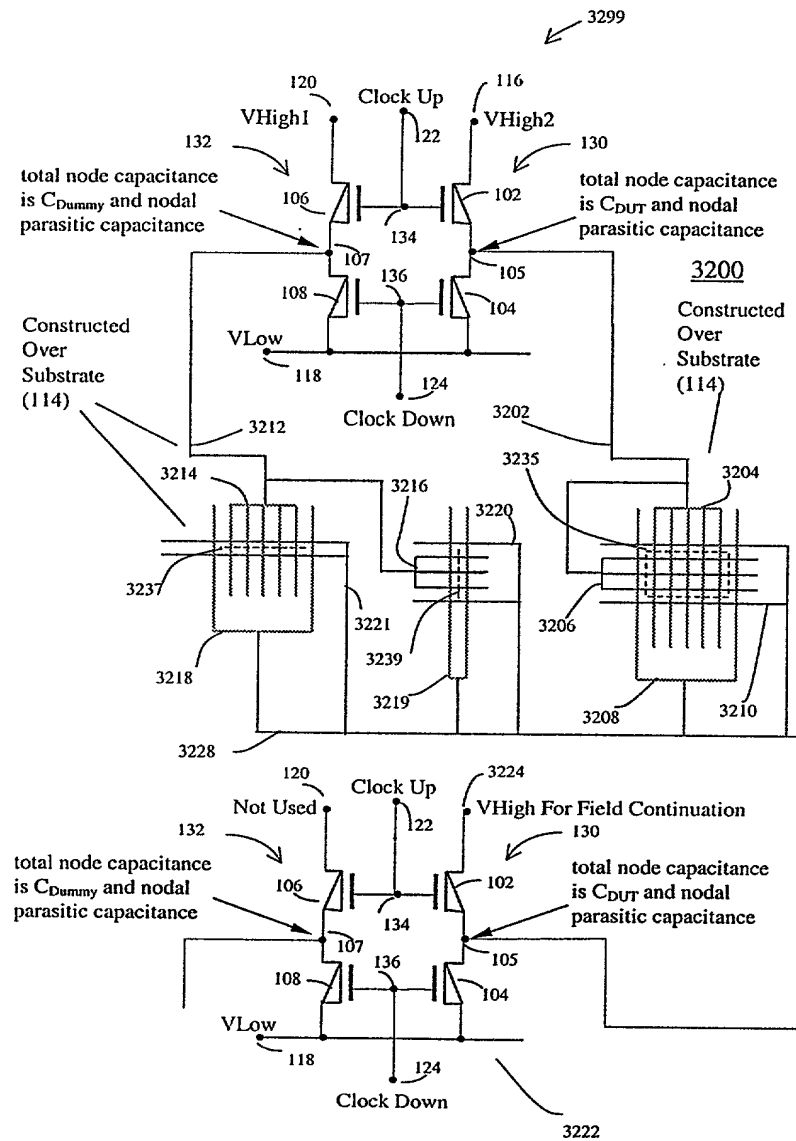
FIG.30





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FIG.32



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FIG.33

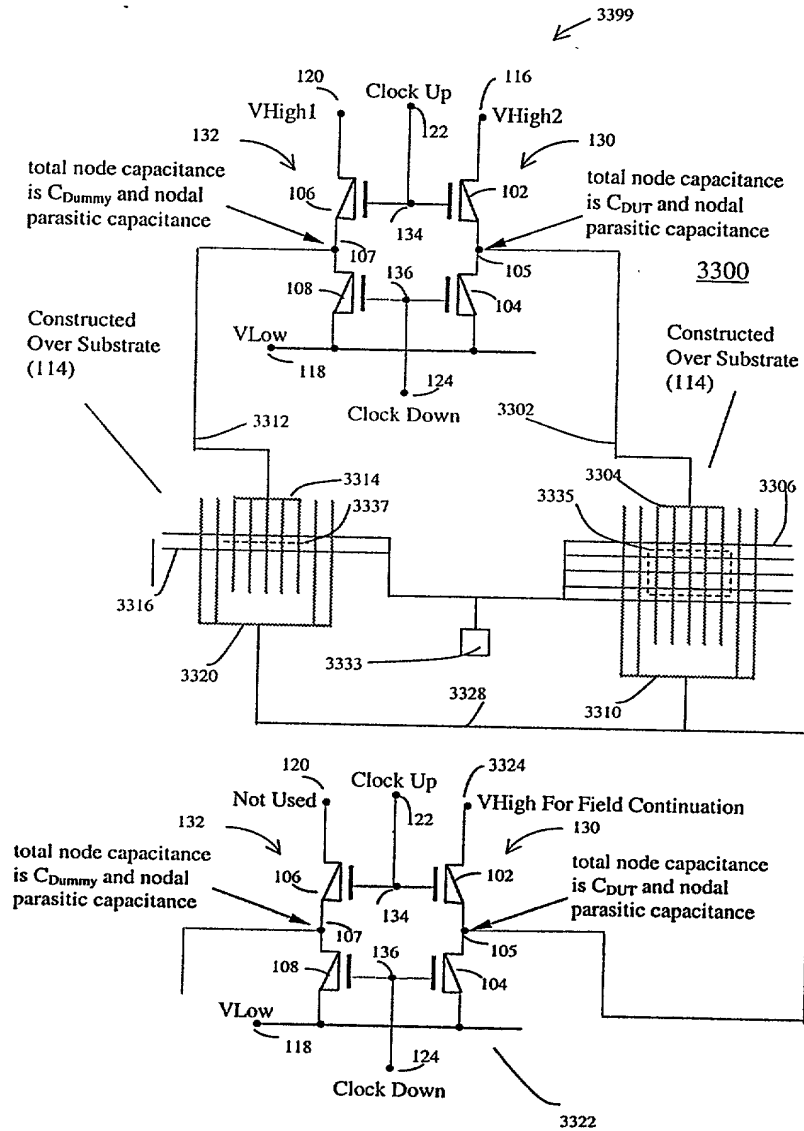
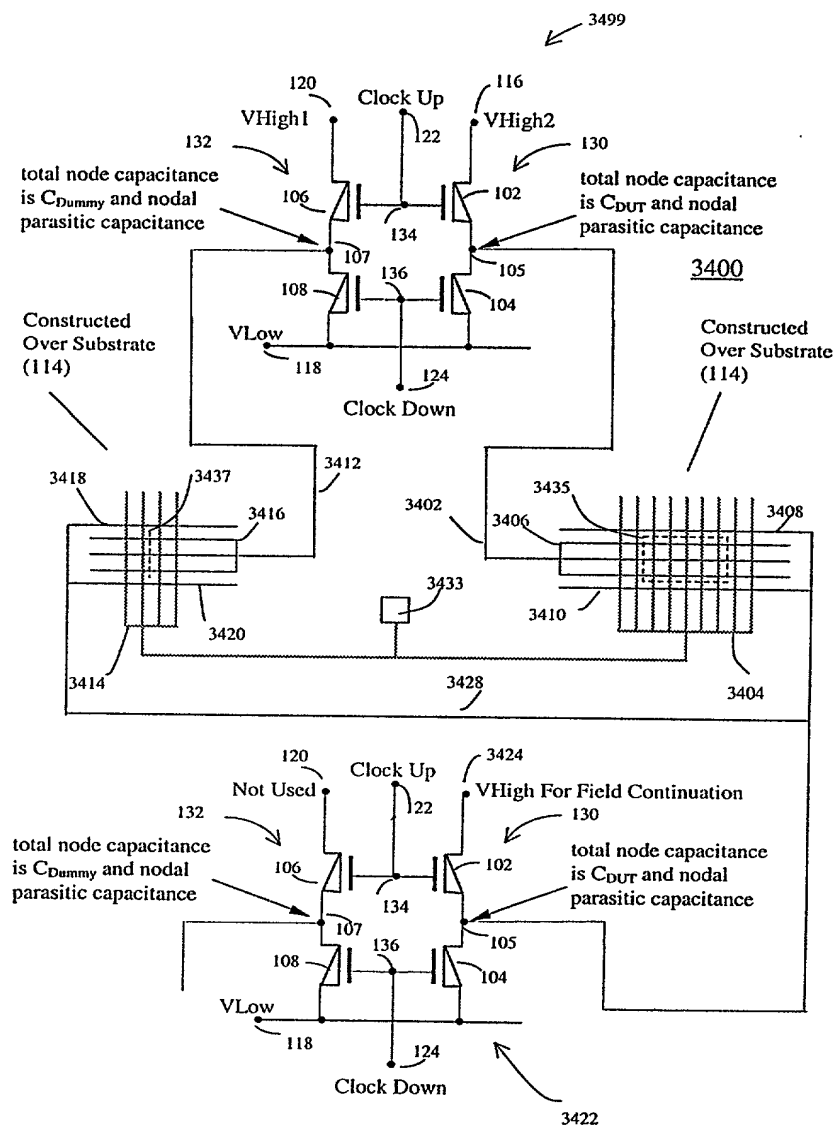
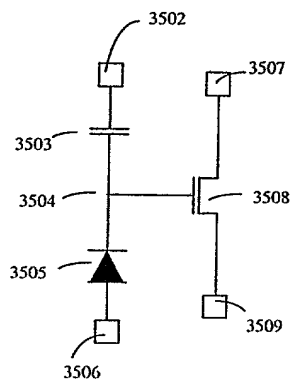


FIG.34



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FIG. 35



3500

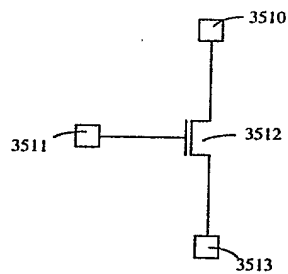
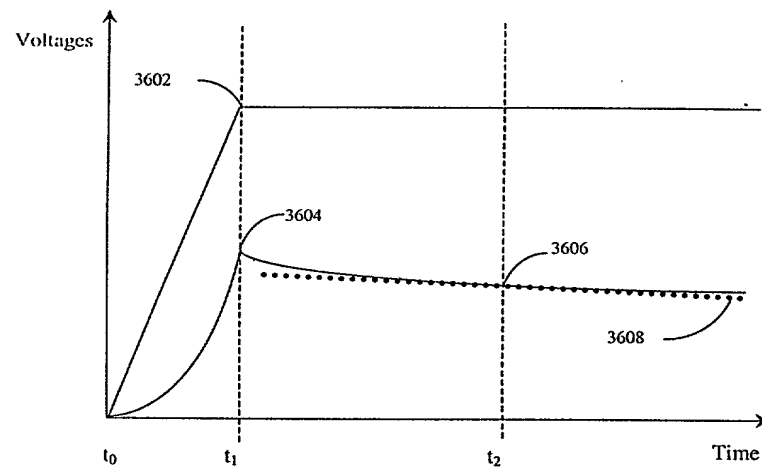


FIG. 36

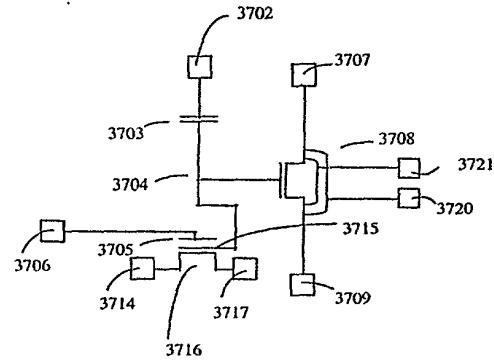
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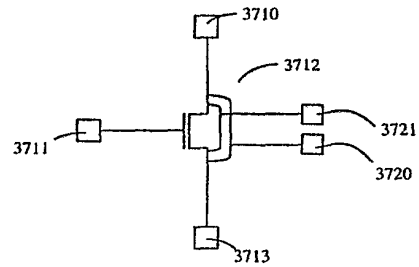
3600

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FIG. 37

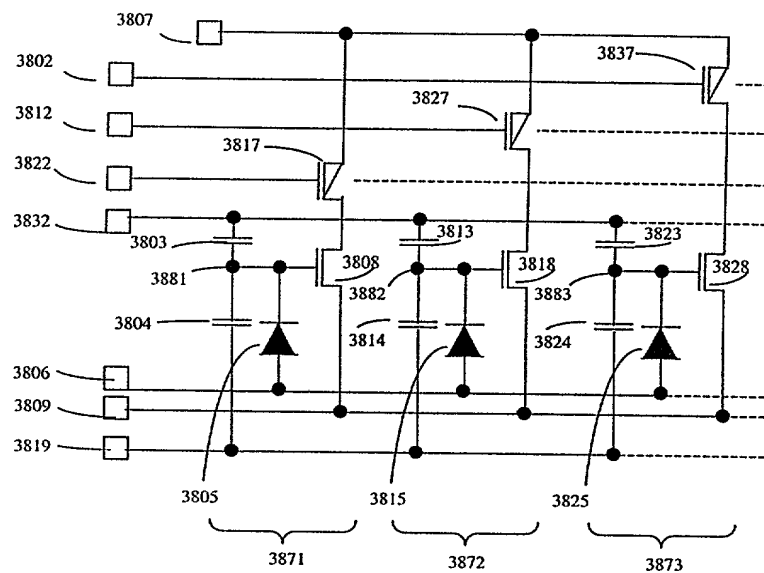


3700



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FIG. 38



3800

